**In Vivado HLS**

* Synthesis Reports:
  + Performance Estimates
  + Utilization Estimates
* Analysis Perspective:
  + schedule in Performance View
  + schedule and resources in Resource View

**In Vivado**

go to directory solution1/impl/verilog and open project project

open Synthesized Design in the Flow Navigator Pane (left window)

* Schematic (logic-level scheme)
* related reports

**Verification**

C-based testbench files for img\_conv\_5x5 design

verification results and reports for img\_conv\_5x5 HLS design both at the C level and RTL level

**Extended HLS Assignment**